

MB-OFDM UWB PHY: Baseband Processor (BBP)

Features

- Supports ECMA-368 PHY requirements for mandatory rates (53.3, 106.7 and 200 Mbps)¹
- Advanced acquisition and channel estimation algorithms to support SNR of < -3 dB
- Streaming mode support
- Low power implementation techniques with advanced clock management logic
- Flexible external interfaces to support a broad range of integration requirements
- Verified against the modified Saleh-Valenzuela multipath model- RMS delay spread up to 25 ns
- Fixed-point performance model implemented in C for maximum design flow flexibility
- RTL verified against fixed-point performance model

Applications

- UWB Wireless Personal Area Networks (WPAN)
 - Short range, low power, very high speed transfer of high-quality multimedia content
 - Computers and peripherals
 - Mobile consumer electronics and communications
- Certified Wireless USB
- Wireless 1394
- High data rate Bluetooth[®] wireless technology
- Wireless HDMI
- Typical consumer scenario
 - Video camcorder, digital camera, and hand held appliance downloads to TV, photo kiosks, and PC
 - Audio/Video distribution for home gaming and entertainment clusters
 - Wireless connectivity between mobile devices and video projection equipment
 - Wireless docking stations

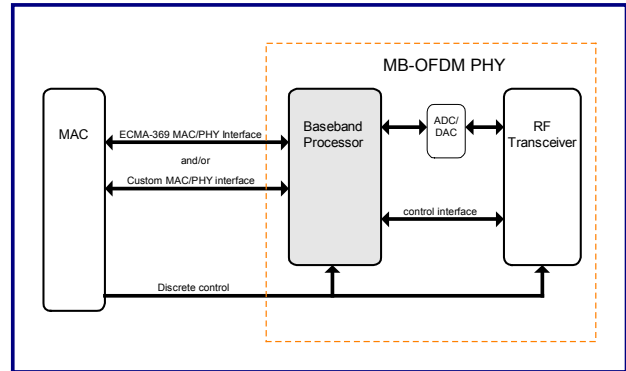


Figure 1: Typical system integration.

Description

The baseband processor provides all functionality to support ECMA-368 including the following:

- Tx/Rx service primitives
- Clear Channel Assessment (CCA)
- Received Signal Strength Indication (RSSI)
- Link Quality Indication (LQI)
- PLCP header with HCS generation
- Power management support

The *aRenarti-SIP* solution also provides services to optimize the following functions to specific transceiver requirements:

- AGC
- DC offset correction
- I/Q imbalance correction
- Multiband signal processing

The *aRenarti-SIP* BBP solution can support either the ECMA-369 MAC-PHY interface or alternate local bus interfaces (e.g.- AMBA AHB). Optional interfaces may be provided to support ASIC as well as FPGA development.

The OFDM baseband processor is a half-duplex device designed to operate in either transmit or receive mode under control of the MAC and its' related

Description (cont.)

protocols. Figure 2 shows a simplified block diagram for the BBP when configured in the receive mode.

Performance

UWB WPAN's provide very high data rate, short range, and low power communications. Typical requirements include an ability to achieve a 200 Mbps information rate at a range of 4 meters and a 110 Mbps information rate at 10 meters. The MB-OFDM waveform provides this level of performance with the ability to both extend the range at lower data rates (ideal for in-home entertainment clusters) and to provide significantly higher data rates at shorter range (PC/Kiosk file transfer). The *aRenarti-SIP* modem provides very robust packet error rate (PER) performance in the multipath environment as shown in Figure 3 (PER vs. E_b/N_o) and Figure 4 (PER vs. Tx/Rx distance). The indicated range performance is based on 0 dB link margin simulations using the modified Saleh-Valenzuela channel model with shadowing (i.e.- a realistic UWB model).

Availability

The fixed-point performance model is currently available. RTL development targeting an FPGA prototyping environment is ongoing. ASIC development work will be performed per customer demand.

Partners In Innovation!

The MB-OFDM modem described herein may be modified to meet the most powerful evolutions of existing technologies as well as a broad range of potentially disruptive new applications. Today we see OFDM modems being deployed in a host of wired and wireless applications including wireless HDMI, mobile TV, 4G cellular, WLAN, WMAN, WPAN, DSL and BPL...just to mention a few. In anticipation of a potential explosion in new research activity, *aRenarti-SIP* has developed the *Partners In Innovation!* program making our high valued IP portfolio available to select partners involved in innovative communications research. We encourage all organizations to inquire about this exciting new licensing program.

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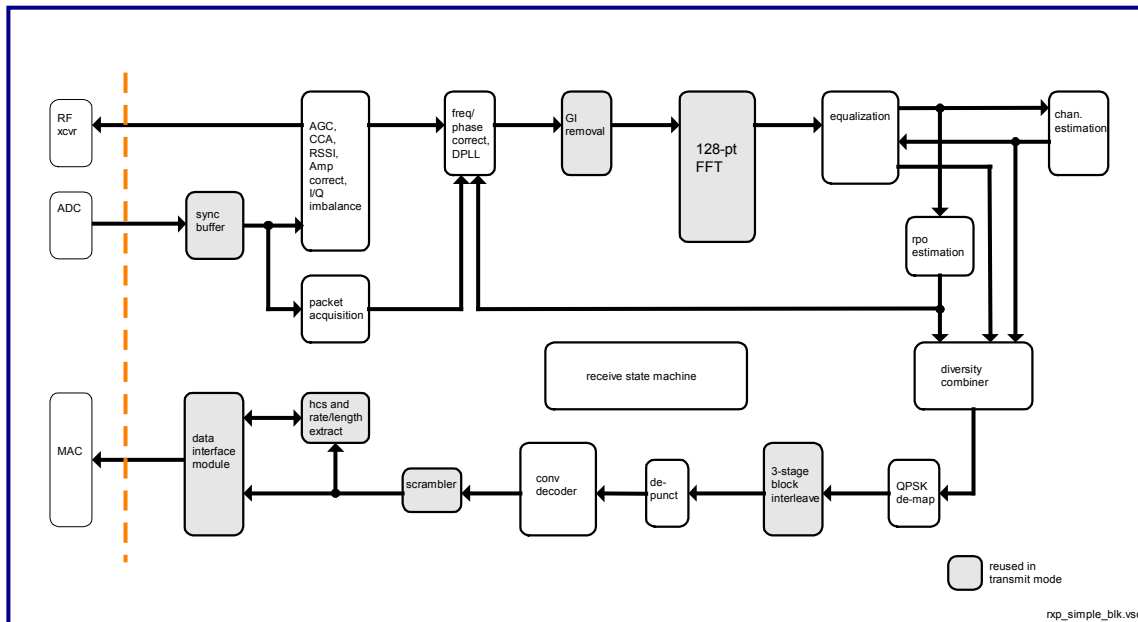


Figure 2: Receive processor simplified block diagram.

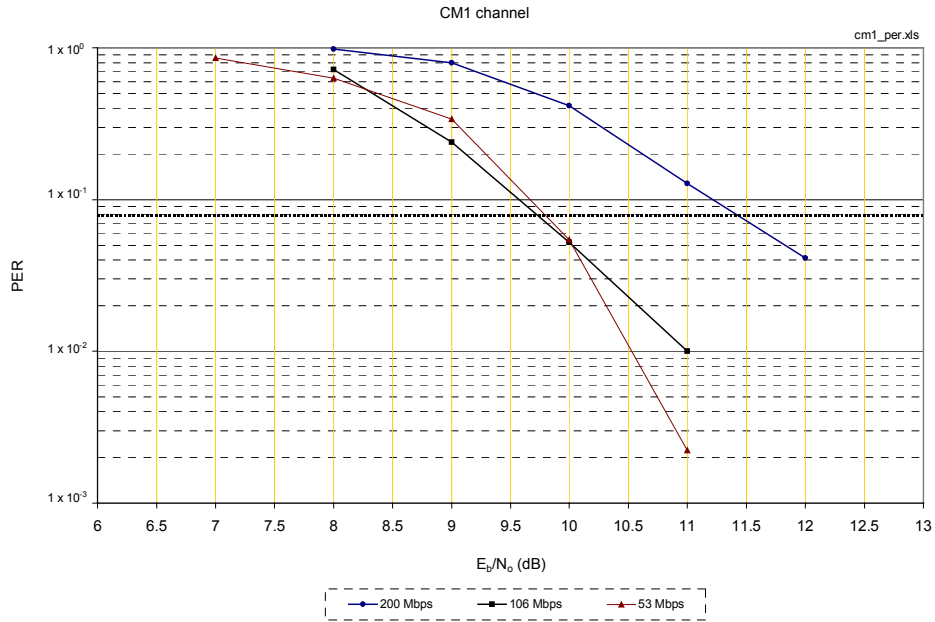


Figure 3: PER vs. E_b/N_0 - CM1 channel.

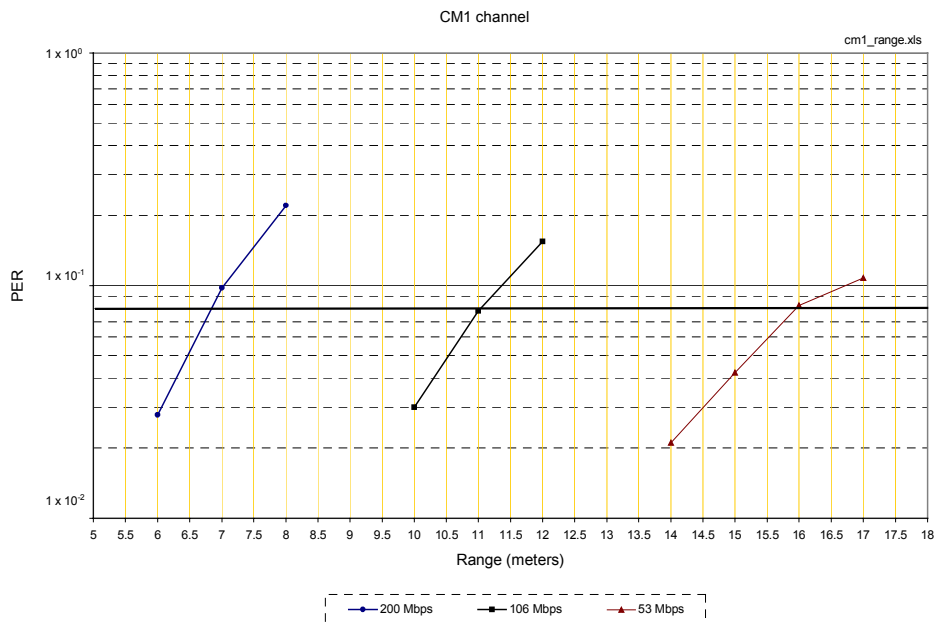


Figure 4: PER vs. range- CM1 channel.

Notes:

1. The performance model provides all data rates identified in the ECMA-368 standard. The higher data rates (320, 400, and 480 Mbps) are implemented with QPSK modulation versus the new, higher order, modulation identified in the standard. With the exception of the convolutional decoder the hardware architecture is designed to support the full 480 Mbps data rate.